UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/074,227	02/14/2002	Takashi Miida		6199

7590 02/25/2003

LORUSSO & LOUD
3137 Mount Vernon Avenue
Alexandria, VA 22305

EXAMINER
YAM, STEPHEN K

ART UNIT	PAPER NUMBER
2878	

DATE MAILED: 02/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/074,227	MIIDA, TAKASHI
	Examiner	Art Unit
	Stephen Yam	2878

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12-16* is/are rejected.

7)☒ Claim(s) *11 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 June 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *7* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 12 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Kozlowski et al. US Patent No. 5,892,540.

Regarding Claim 12, Kozlowski et al. teach (see Fig. 1) a solid-state imaging device comprising a plurality (12) of photoelectric conversion devices arrayed in rows and columns (see Col. 5, lines 43-55) for converting an optical signal into an electric signal and outputting the electric signal, an amplifier (22) for each of the columns (see Col. 5, lines 22-24) for sequentially inputting a first signal voltage (see Col. 6, lines 44-46) and a second signal voltage obtained by initializing (reset) the photoelectric conversion device (see Col. 6, lines 45-48), converting the first and second signal voltage into charges (see Col. 6, lines 40-53), and outputting a difference signal (inherent within a correlated-double-sampling process- see below) (see Col. 6, lines 40-42) between the first and second signal voltage, a video signal output terminal ("OUTPUT") for outputting the difference signal as a video signal corresponding to the optical signal (see Col. 4, lines 34-36), and a switching means (see Col. 7, lines 27-36) between the amplifiers of at least two columns for mixing the difference signals of at least two columns. Regarding the sequential inputting of a first and second voltage and outputting a difference signal, a correlated-double-sampling (CDS) operation for an imaging system is performed by inputting a first signal as a

base signal, inputting a second signal after the first signal as the sampling signal, and outputting the difference between the two signals to cancel DC offset or noise (characteristic of the base signal) within the imaging system.

Regarding Claim 15, Kozlowski et al. teach a method of a solid-state imaging device with a plurality (12) of photoelectric conversion devices arrayed in rows and columns (see Col. 5, lines 43-55) for converting an optical signal into an electric signal and outputting the electric signal, a plurality of amplifiers (22) for the respective columns (see Col. 5, lines 22-24) for sequentially inputting a first signal voltage (see Col. 6, lines 44-46) and a second signal voltage obtained by initializing (reset) the photoelectric conversion device (see Col. 6, lines 45-48), converting the first and second signal voltage into charges (see Col. 6, lines 40-53), and outputting a difference signal (inherent within a correlated-double-sampling process) (see Col. 6, lines 40-42) therebetween, and a video signal output terminal ("OUTPUT") for outputting the difference signal as a video signal corresponding to the optical signal (see Col. 4, lines 34-36), the method comprising mixing (see Col. 7, lines 27-36) the difference signals from the amplifiers of at least two columns, and outputting an output signal (output from (22)) from the amplifier.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gregorian et al. US Patent No. 4,555,668.

Regarding Claims 1 and 2, Gregorian et al. teach (see Fig. 3) a variable gain amplifier comprising an input terminal (115) for sequentially inputting a first signal voltage (V_{off100}) (see Col. 4, lines 40-63) and a second signal voltage (V_{in}) (see Col. 5, lines 20-22), an output terminal (140) for outputting (see Col. 5, lines 22-35) a difference signal $V_{140}(t_3)$ between the first and second signal voltages, an operational amplifier (120) including a positive input terminal to which a reference voltage (ground) is inputted, a negative input terminal (115) connected through a signal path to the input terminal of the variable gain amplifier and an output terminal (140) connected to the output terminal of the variable gain amplifier, an input capacitor (110) provided in the signal path having one end connected to the input terminal of the variable gain amplifier and the other end connected to the negative input terminal of the operational amplifier, a feedback capacitor (130) provided between the negative input terminal and the output terminal of the operational amplifier, a first switch device (ϕ_3) for connecting or disconnecting the signal path, a second switch device (20 / ϕ_2) for connecting or disconnecting an input of the reference voltage to the one end of the input capacitor, and a third switch device (125 / ϕ_1) for connecting or disconnecting the negative input terminal and the output terminal of the operational amplifier. Regarding Claim 2, Gregorian et al. also teach a variable capacitor (110) having a plurality of capacitors (110-1, 110-2, 110-3, etc.) and switch devices (110-2a, 110-3a, etc.) for providing an adjustable capacitance. Gregorian et al. do not teach the feedback capacitor as a variable-set capacitor. It is design choice to use a variable feedback capacitor in place of a variable input capacitor, as both designs provide the ability to alter the gain of the amplifier, equal to

$C_{input}/C_{feedback}$. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a variable feedback capacitor in place of a variable input capacitor in the amplifier of Gregorian et al., to optimize the placement of components on a circuit board or IC chip.

5. Claims 3, 6, 8, 9, 10, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kozlowski et al. in view of Satoh US Patent No. 6,342,694.

Regarding Claim 3, Kozlowski et al. teach (see Fig. 1) a variable gain amplifier (24) outputting a difference signal (inherent within a correlated-double-sampling process) (see Col. 6, lines 40-42) between a first and second signal voltage, wherein the first and second signal voltage are sequentially inputted (see Col. 6, lines 44-48) and converted to charges (see Col. 6, lines 40-53) to generate a difference signal (inherent within a correlated-double-sampling process) (see Col. 6, lines 40-42). Kozlowski et al. do not teach adjusting the gain according to the difference signal and outputting an adjusted difference signal. Satoh teaches (see Fig. 9) an amplifier (3) for a photodiode (1) wherein the gain of the amplifier is adjusted (see Col. 5, lines 33-42) based on the amplitude of a difference signal (out of (14)) between a first (V_{OUT} stored in (10)) and second signal (V_{REF} stored in (12)), and hence outputting an adjusted output (see Col. 5, lines 41-43). It would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the gain of the amplifier according to the difference signal as taught by Satoh in the method of Kozlowski et al., to provide real-time adjustment of a dynamic range to enable linear amplifier gain for accurate amplification.

Regarding Claim 6, Kozlowski et al. teach (see Fig. 1) a solid-state imaging device comprising a plurality (12) of photoelectric conversion devices arrayed in rows and columns (see Col. 5, lines 43-55) for converting an optical signal into an electric signal and outputting the electric signal, an amplifier (22) for each of the columns (see Col. 5, lines 22-24) for sequentially inputting a first signal voltage (see Col. 6, lines 44-46) and a second signal voltage obtained by initializing (reset) the photoelectric conversion device (see Col. 6, lines 45-48), converting the first and second signal voltage into charges (see Col. 6, lines 40-53), and outputting a difference signal (inherent within a correlated-double-sampling process) (see Col. 6, lines 40-42) between the first and second signal voltage. Kozlowski et al. do not teach adjusting the gain according to the difference signal and outputting an adjusted difference signal. Satoh teaches (see Fig. 9) an amplifier (3) for a photodiode (1) wherein the gain of the amplifier is adjusted (see Col. 5, lines 33-42) based on the amplitude of a difference signal (out of (14)) between a first (V_{OUT} stored in (10)) and second signal (V_{REF} stored in (12)), and hence outputting an adjusted output (see Col. 5, lines 41-43). It would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the gain of the amplifier according to the difference signal as taught by Satoh in the method of Kozlowski et al., to provide real-time adjustment of a dynamic range to enable linear amplifier gain for accurate amplification.

Regarding Claims 8 and 9, Kozlowski et al. teach (see Fig. 1) an optical signal reading method comprising irradiating a photoelectric conversion device (14) with an optical signal, outputting a first signal voltage obtained by converting the optical signal into an electric signal, converting (see Col. 6, lines 44-46) the first signal voltage into charges and storing the charges, outputting (see Col. 6, lines 45-48) a second signal charge at an initialization (reset) of the

photoelectric conversion device, converting (see Col. 6, lines 49-51) the second signal voltage into charges (in the capacitor), generating a difference signal (inherent within a correlated-double-sampling process) (see Col. 6, lines 40-42) between the first signal voltage and the second signal voltage, and converting (see Col. 4, lines 2-7) the difference signal into a digital signal. Kozlowski et al. also teach a gain-adjustable amplifier (22) and altering the gain of the amplifier for each frame (see Col. 3, lines 17-20). Regarding Claim 9, Kozlowski et al. teach (see Fig. 1) a plurality (12) of photoelectric conversion devices arrayed in rows and columns (see Col. 5, lines 43-55) and the difference signal is outputted for each column (20) (see Col. 5, lines 22-24 and 44-55). Kozlowski et al. do not teach adjusting the gain according to the difference signal and outputting an adjusted difference signal. Satoh teaches (see Fig. 9) an amplifier (3) for a photodiode (1) wherein the gain of the amplifier is adjusted (see Col. 5, lines 33-42) based on the amplitude of a difference signal (out of (14)) between a first (V_{OUT} stored in (10)) and second signal (V_{REF} stored in (12)), and hence outputting an adjusted output (see Col. 5, lines 41-43). It would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the gain of the amplifier according to the difference signal as taught by Satoh in the method of Kozlowski et al., to provide real-time adjustment of a dynamic range to enable linear amplifier gain for accurate amplification.

Regarding Claim 13, Kozlowski et al. teach the method as taught in Claim 12, according to the appropriate paragraph above. Kozlowski et al. also teach a gain-adjustable amplifier (22) and altering the gain of the amplifier for each frame (see Col. 3, lines 17-20). Kozlowski et al. do not teach adjusting the gain according to the difference signal and outputting an adjusted difference signal. Satoh teaches (see Fig. 9) an amplifier (3) for a photodiode (1) wherein the

gain of the amplifier is adjusted (see Col. 5, lines 33-42) based on the amplitude of a difference signal (out of (14)) between a first (V_{OUT} stored in (10)) and second signal (V_{REF} stored in (12)), and hence outputting an adjusted output (see Col. 5, lines 41-43). It would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the gain of the amplifier according to the difference signal as taught by Satoh in the method of Kozlowski et al., to provide real-time adjustment of a dynamic range to enable linear amplifier gain for accurate amplification.

Regarding Claims 10 and 14, Kozlowski et al. in view of Satoh teach the method as taught in Claims 9 and 13, according to the appropriate paragraph above. Kozlowski et al. also teach (see Fig. 1) each of the photoelectric conversion devices (12) comprising a photodetector (14) and a field effect transistor (16) provided adjacently to the photodetector to output a first and second signal voltage for correlated doubling sampling. Kozlowski et al. do not teach the field effect transistor as having an insulated gate with a heavily doped buried layer around a source region under a channel region below a gate electrode. It is well known in the art to construct a photodetector using a heavily doped source layer to provide specific current-channel characteristics and use a gate electrode above the source and drain regions to control the current flow. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a heavily doped source layer and a gate electrode in the device of Kozlowski et al. in view of Satoh, to provide specific current and voltage characteristics for efficiently outputting the electrical signal converted by the photodetector.

6. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kozlowski et al.

Kozlowski et al. teach the method as taught in Claim 15, according to the appropriate paragraph above. Kozlowski et al. also teach (see Fig. 1) each of the photoelectric conversion devices (12) comprising a photodetector (14) and a field effect transistor (16) provided adjacently to the photodetector to output a first and second signal voltage for correlated doubling sampling. Kozlowski et al. do not teach the field effect transistor as having an insulated gate with a heavily doped buried layer around a source region under a channel region below a gate electrode. It is well known in the art to construct a photodetector using a heavily doped source layer to provide specific current-channel characteristics and use a gate electrode above the source and drain regions to control the current flow. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a heavily doped source layer and a gate electrode in the device of Kozlowski et al., to provide specific current and voltage characteristics for efficiently outputting the electrical signal converted by the photodetector.

7. Claims 4, 5, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gregorian et al. in view of Kozlowski et al.

Regarding Claim 4, Gregorian et al. teaches or makes obvious all the claim limitations with respect to the amplifier components, as explained above for Claim 1. Gregorian et al. do not teach a plurality of photoelectric conversion devices arrayed in rows and columns or an analog/digital conversion circuit for converting the difference signal into a digital signal. Kozlowski et al. teach (see Fig. 1) an imager with a plurality of photoelectric conversion devices (12) arrayed in rows and columns (see Col. 5, lines 43-55) leading to an amplifier (24) for sequentially inputting (see Col. 6, lines 44-48) a first and second signal voltage and generating a

difference signal (inherent within a correlated-double-sampling process) (see Col. 6, lines 40-42) and a analog/digital conversion circuit (see Col. 4, lines 5-7) for converting the output of the amplifier to a digital signal. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the device of Gregorian et al. for the imager of Kozlowski et al., to provide efficient storage of a first signal within the amplifier for comparison with a second signal.

Regarding Claim 5, Gregorian et al. in view of Kozlowski et al. teach the device as taught in Claim 4, according to the appropriate paragraph above. Gregorian et al. also teach a variable capacitor (110) having a plurality of capacitors (110-1, 110-2, 110-3, etc.) and switch devices (110-2a, 110-3a, etc.) for providing an adjustable capacitance. Gregorian et al. do not teach the feedback capacitor as a variable-set capacitor. It is design choice to use a variable feedback capacitor in place of a variable input capacitor, as both designs provide the ability to alter the gain of the amplifier, equal to $C_{input}/C_{feedback}$. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a variable feedback capacitor in place of a variable input capacitor in the device of Gregorian et al. in view of Kozlowski et al., to optimize the placement of components on a circuit board or IC chip.

Regarding Claim 7, Gregorian et al. in view of Kozlowski et al. teach the device as taught in Claim 4, according to the appropriate paragraph above. Kozlowski et al. also teach (see Fig. 1) each of the photoelectric conversion devices (12) comprising a photodetector (14) and a field effect transistor (16) provided adjacently to the photodetector to output a first and second signal voltage for correlated doubling sampling. Gregorian et al. and Kozlowski et al. do not teach the field effect transistor as having an insulated gate with a heavily doped buried layer around a

source region under a channel region below a gate electrode. It is well known in the art to construct a photodetector using a heavily doped source layer to provide specific current-channel characteristics and use a gate electrode above the source and drain regions to control the current flow. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a heavily doped source layer and a gate electrode in the device of Gregorian et al. in view of Kozlowski et al., to provide specific current and voltage characteristics for efficiently outputting the electrical signal converted by the photodetector.

Allowable Subject Matter

8. Claims 11 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: The amplifier as claimed, specifically in combination with the method of connecting and disconnecting the appropriate switches to store charges from the first signal voltage in the input capacitor, transfer it to the feedback capacitor, read a second signal voltage, generate a difference signal between the first and the second signals, and adjust the gain of the amplifier according to the difference signal, is not disclosed or made obvious by the prior art of record.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Haque et al. US Patent No. 4,438,354, teach an amplifier with adjustable gain and a first, second, and third switch, and outputting a difference between two voltage signals.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen Yam whose telephone number is (703)306-3441. The examiner can normally be reached on Monday-Friday 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Porta can be reached on (703)308-4852. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7724 for regular communications and (703)308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

SY
February 19, 2003

DAVID PORTA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800